REMARKS

Claims 39, 41 and 44-52 are cancelled. New claims 53-67 are added. Claims 53-67 are pending in the application.

Claims 39, 41, and 44-52 stand rejected under numerous grounds as set forth in the present Action. Without admission as to the propriety of any of the Examiner's rejections, claims 39, 41, and 44-52 are cancelled.

New claims 53-67 do not add "new matter" to the application since each is fully supported by the specification as originally filed. Claims 53 and 60 are supported by the specification at, for example, page 11, lines 18-20; and the claims as originally filed. Claims 54-56 are supported by the specification at, for example, page 10, lines 13-20. Claim 57 is supported by the specification at, for example, page 11, lines 9-20. Claims 58 and 67 are supported by the specification a, for example, page 9, lines 8-12. Claim 59 is supported by the specification at, for example, page 11, lines 9-20. Claim 61 is supported by the specification at, for example, page 11, line 21 through page 12, line 13; and page 12, lines 19-20. Claims 62-63 are supported by the specification at, for example, page 10, lines 3-18. Claim 64 is supported by the specification at, for example, page 12, lines 2-13. Claim 65 is supported by the specification at, for example, page 11, lines 18-20. Claim 66 is supported by the specification at, for example, page 4, lines 4-5.

For the reasons discussed above claims 53-67 are believed allowable. Accordingly, Applicant requests examination and allowance of claims 53-67 in the Examiner's next Action.

Applicant acknowledges the Examiner's non-consideration of the Japan patent listed on the Information Disclosure Statement filed by Applicant on December 15, 1998, due to the lack of translation. Applicant submits herewith a Supplemental IDS submitting the English translation of the abstract of such patent and respectfully requests consideration of such abstract by the Examiner during the examination of pending claims 53-67.

Respectfully submitted,

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Examiner ..... Kielin, Erik J.
Attorney's Docket No. MI22-1098
Title: Semiconductor Processing Methods of Chemical Vapor Depositing SiO2 on a Substrate

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO APRIL 19, 2002 OFFICE ACTION

In the Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

Claims 39, 41 and 44-52 are cancelled.

53. (New) A semiconductor processing method of depositing SiO_2 on a substrate comprising:

providing a substrate within a chemical vapor deposition reactor;

forming a liquid mixture comprising an organic silicon precursor and at least one of H_2O and H_2O_2;

converting the liquid mixture into a gaseous mixture;

feeding the gaseous mixture into the chemical vapor deposition reactor; and

utilizing the gaseous mixture, depositing a layer of SiO_2 on the substrate at a rate of about 7000 Å per minute

54. (New) The semiconductor processing method of claim 53 wherein the liquid mixture comprises no less than about 0.5% by volume of the at least one of H_2O and H_2O_2.

55. (New) The semiconductor processing method of claim 53 wherein the liquid mixture comprises from about 5% to about 15% by volume of the at least one of H_2O and H_2O_2.

56. (New) The semiconductor processing method of claim 53 wherein the converting comprises heating the liquid to a temperature of from about 65°C to about 80°C.

57. (New) The semiconductor processing method of claim 53 wherein the chemical vapor deposition reactor is a cold wall low pressure chemical vapor deposition reactor.

58. (New) The semiconductor processing method of claim 53 wherein the silicon precursor is selected from the group consisting of: tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclo-tetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).

59. (New) The semiconductor processing method of claim 53 wherein during the depositing the reactor comprises an internal pressure of from about 10 Torr to about 80 Torr.

60. (New) A semiconductor processing method of depositing SiO_2 on a substrate comprising:

providing a substrate within a chemical vapor deposition reactor;

feeding a gaseous silicon precursor into the chemical vapor deposition reactor;

feeding gaseous H_2O_2 into the chemical vapor deposition reactor; and

utilizing the silicon precursor, depositing a layer of SiO_2 over a surface of the substrate at a rate of about 7000 Å per minute.

61. (New) The semiconductor processing method of claim 60 wherein the gaseous H_2O_2 and the gaseous silicon precursor are fed into the chemical vapor deposition reactor independently.

62. (New) The semiconductor processing method of claim 60 wherein the gaseous H_2O_2 and the gaseous silicon precursor are fed into the chemical vapor deposition reactor simultaneously.

63. (New) The semiconductor processing method of claim 60 wherein the gaseous H_2O_2 and the gaseous silicon precursor are combined prior to feeding into the chemical vapor deposition reactor.

64. (New) The semiconductor processing method of claim 60 further comprising feeding gaseous H_2O into the chemical vapor deposition reactor.

65. (New) The semiconductor processing method of claim 60 wherein the providing a substrate within a chemical vapor deposition reactor comprises providing a wafer gap to susceptor distance of about 230 mils.

66. (New) The semiconductor processing method of claim 60 wherein the surface of the substrate comprises a high aspect ratio topology and wherein the layer is conformally deposited over the topology.

67. (New) The semiconductor processing method of claim 60, wherein the silicon precursor is selected from the group consisting of: tetraethoxysilane (TEOS), diethylsilane (DES), tetramethylcyclo-tetrasiloxane (TMCTS), fluorotriethoxysilane (FTES), and fluorotrialkoxysilane (FTAS).

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